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Prior art: READ and WRITE cycles

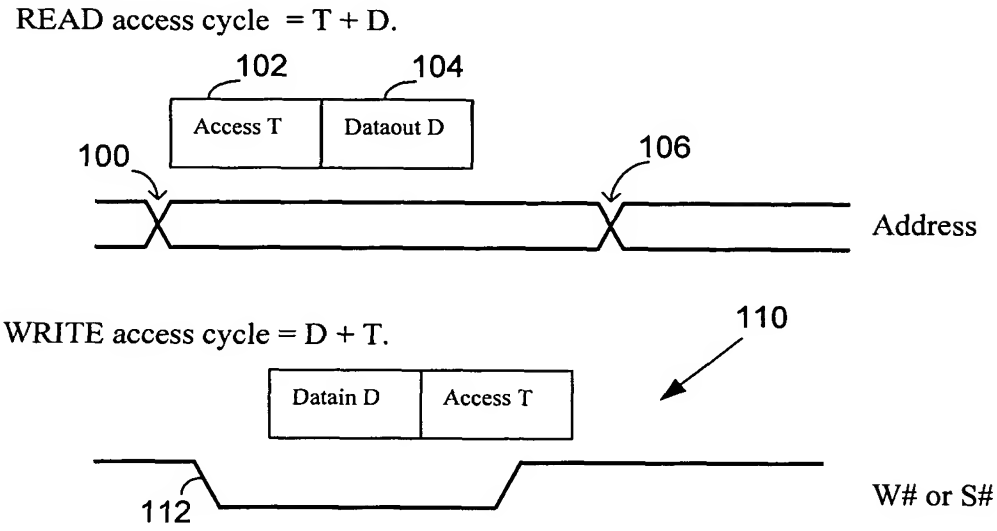

FIG. 1A
PRIOR ART

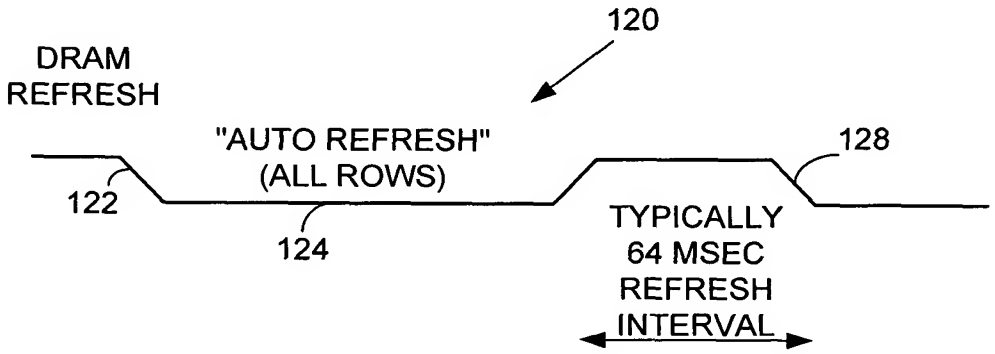

FIG. 1B
PRIOR ART

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READ access cycle = T + T + D:

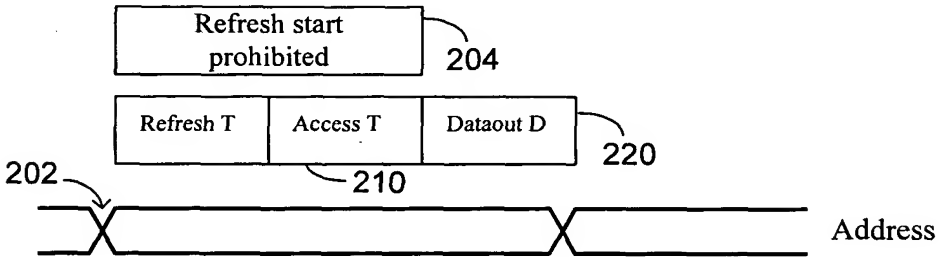

FIG. 2A

WRITE access cycle = D + T + T.

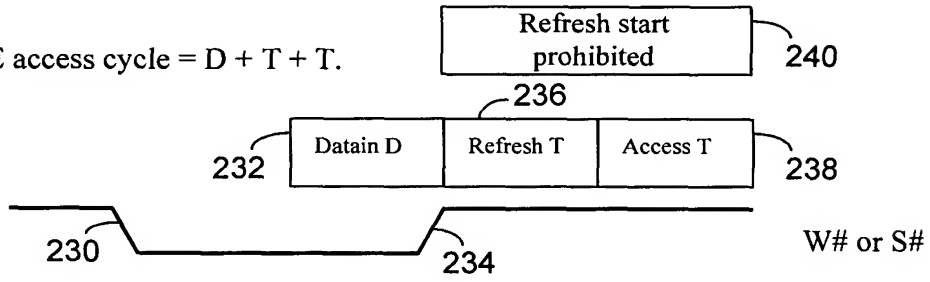

FIG. 2B

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Invalid READ, termination during " dataout"

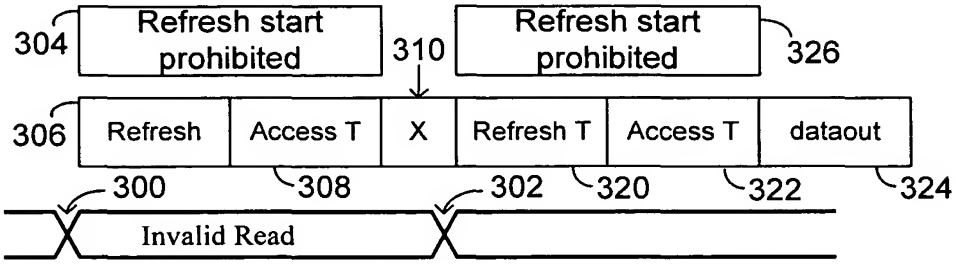

FIG. 3A

Invalid READ, termination during "access"

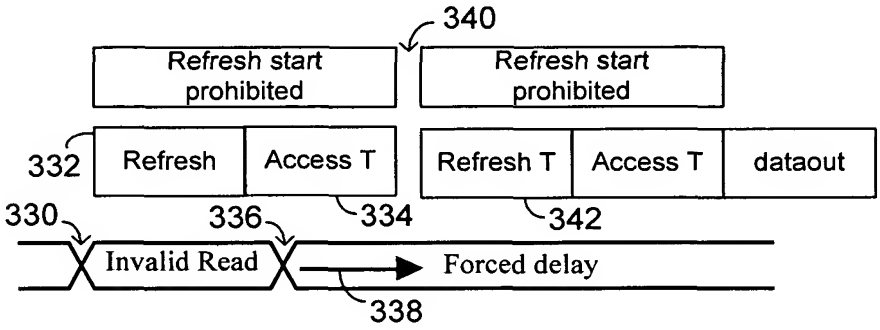

FIG. 3B

Invalid READ, termination during "refresh"

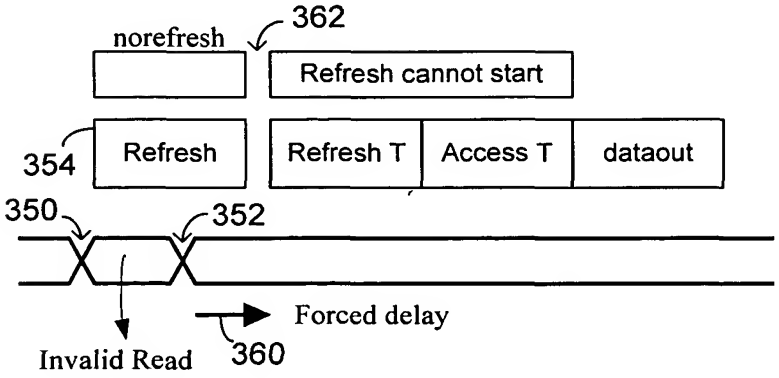

FIG. 3C

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READ access following a WRITE:

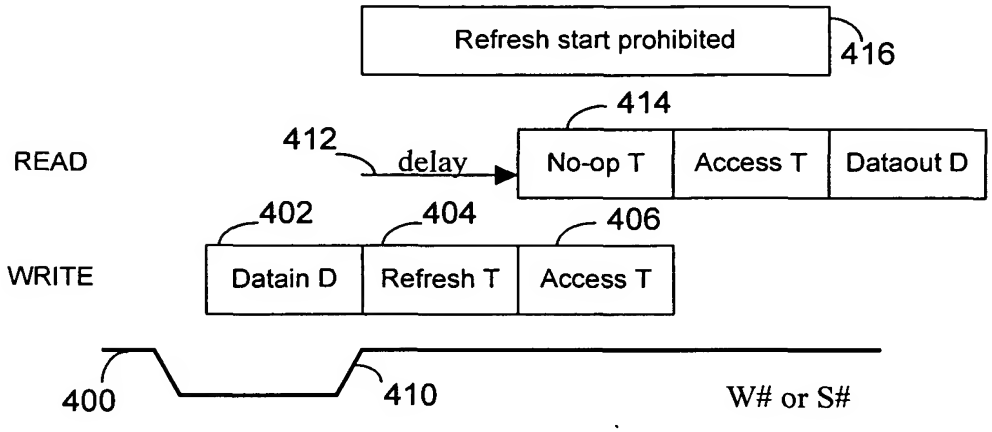

FIG. 4A

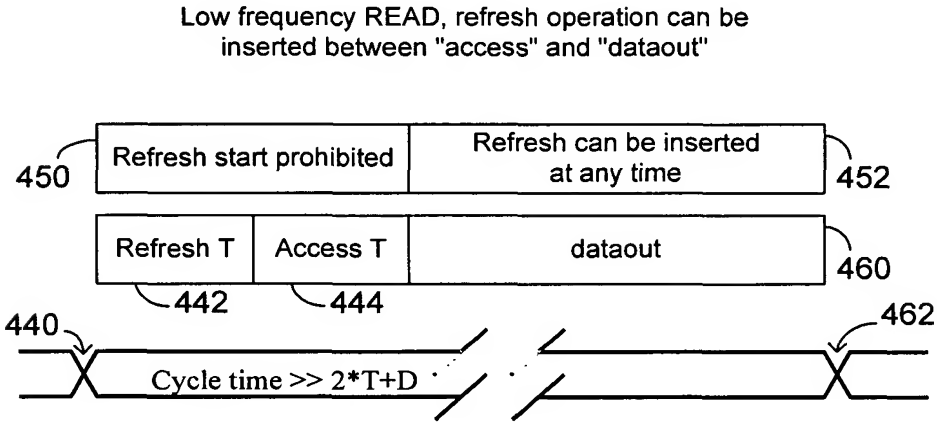

FIG. 4B

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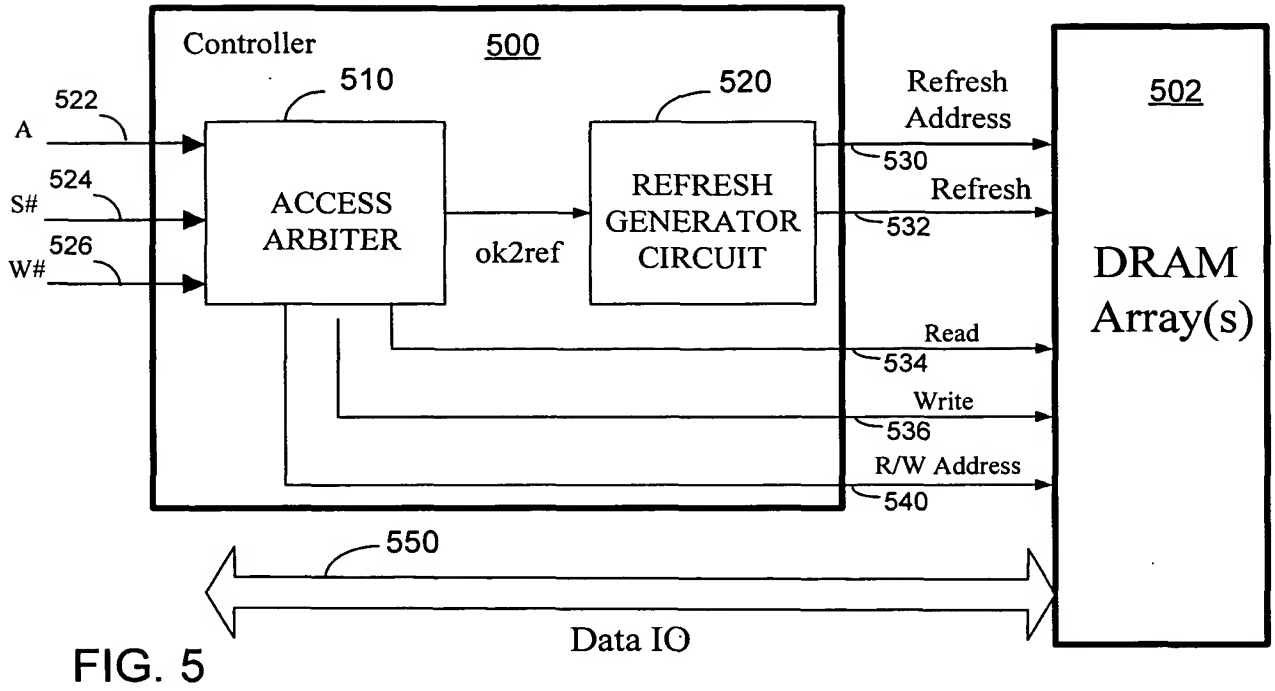

FIG. 5

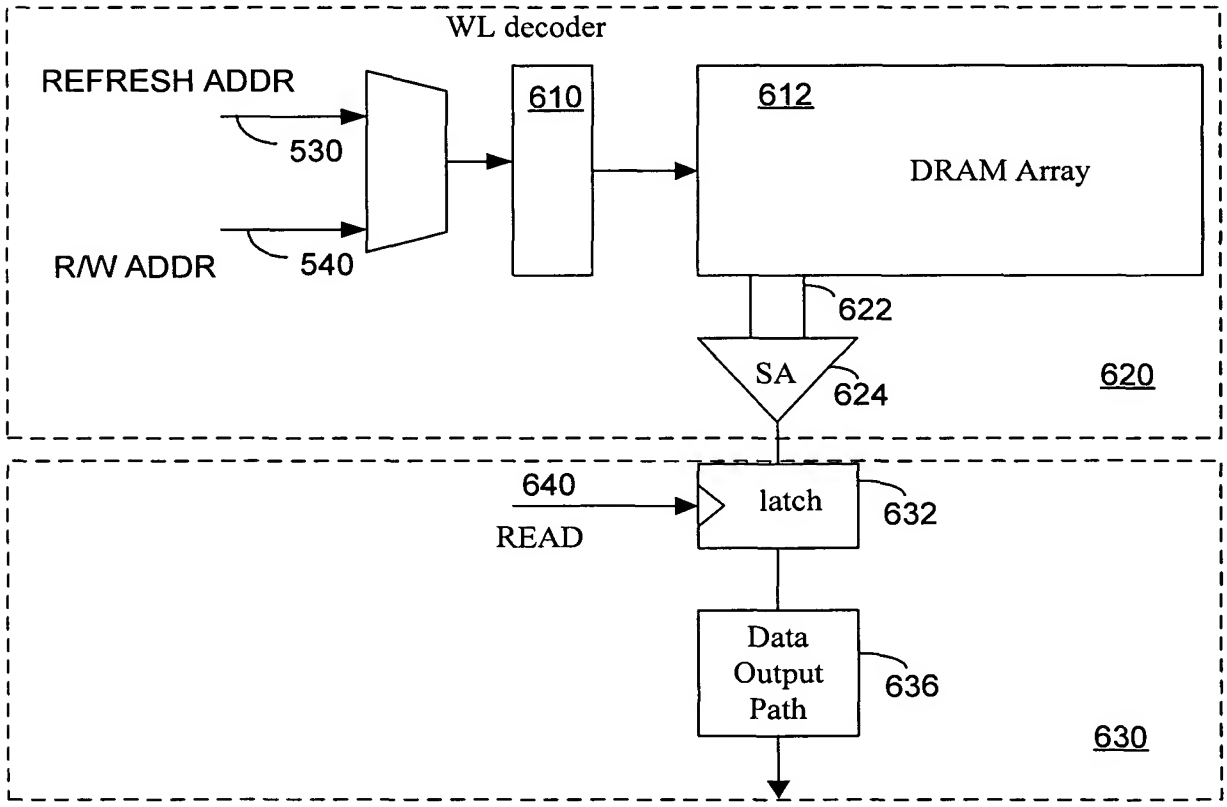

FIG. 6

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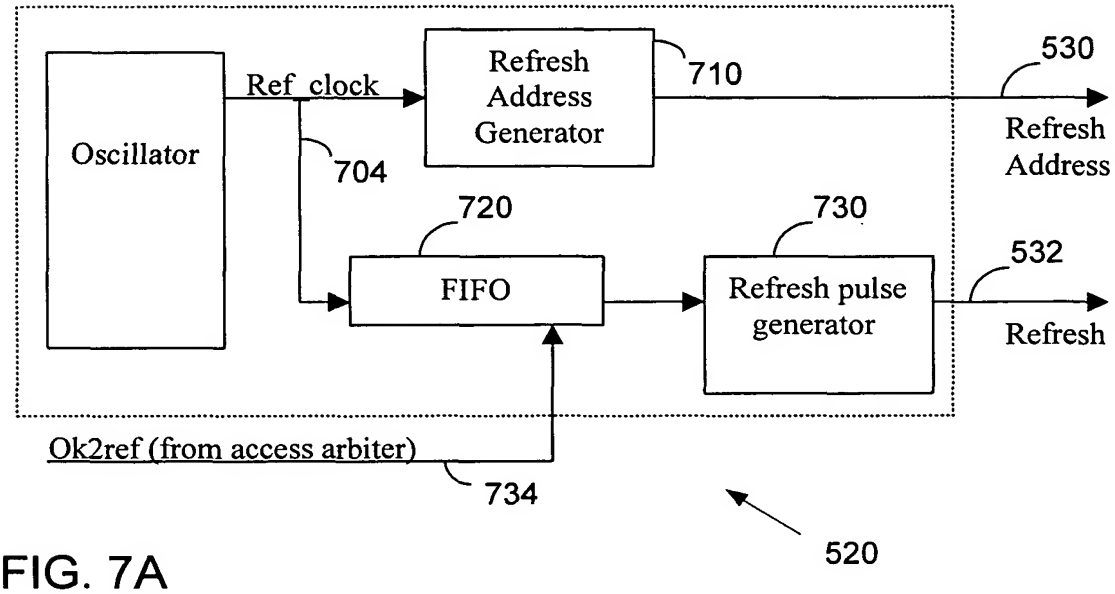

FIG. 7A

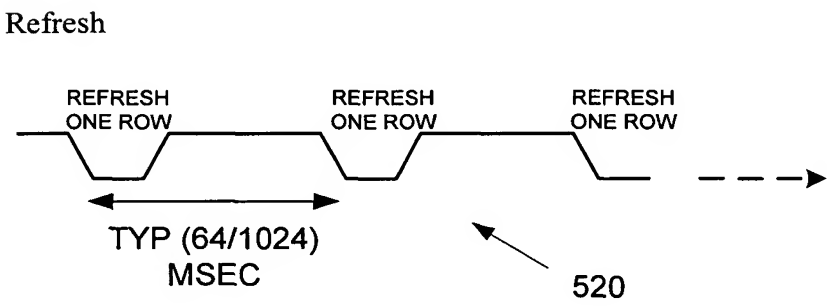

FIG. 7B

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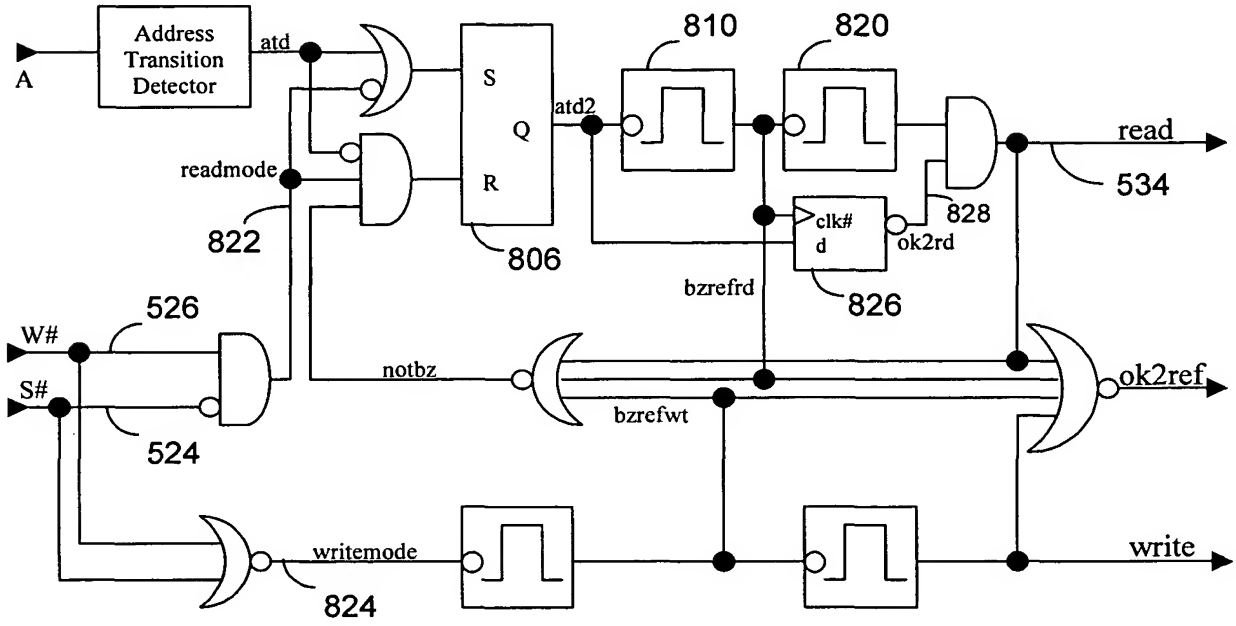
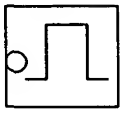


FIG. 8

"FETPG"



Falling edge triggered pulse generator. Falling edge of input triggers a high going pulse of duration T.

Timing diagram for a normal read access

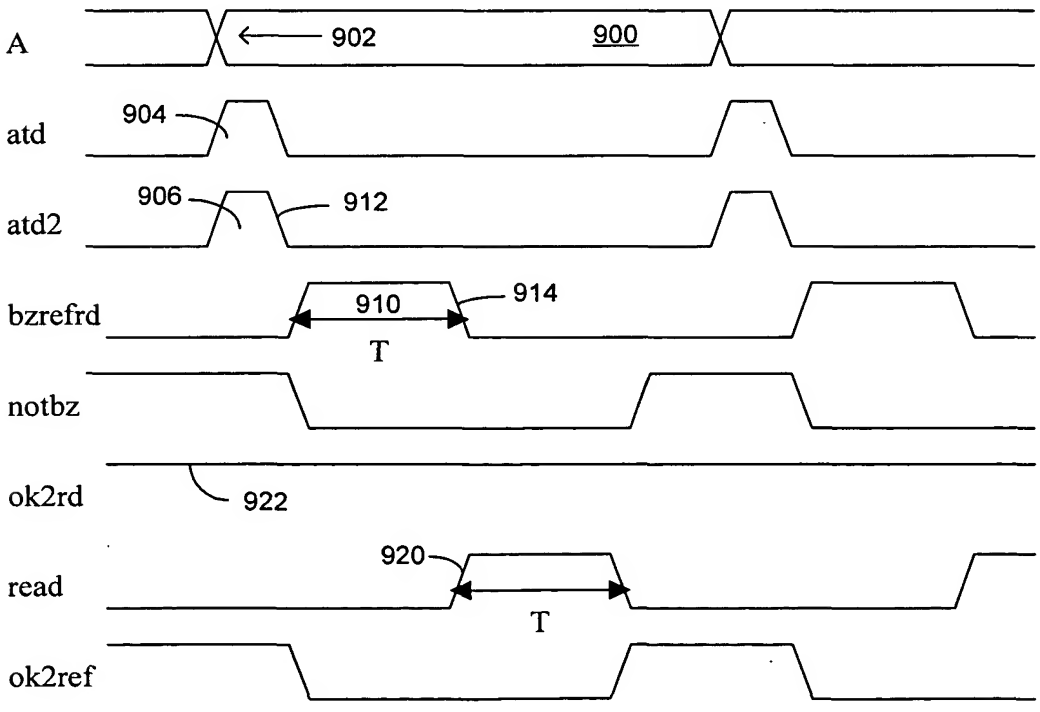


FIG. 9

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Timing diagram for an invalid read operation terminated within T of starting

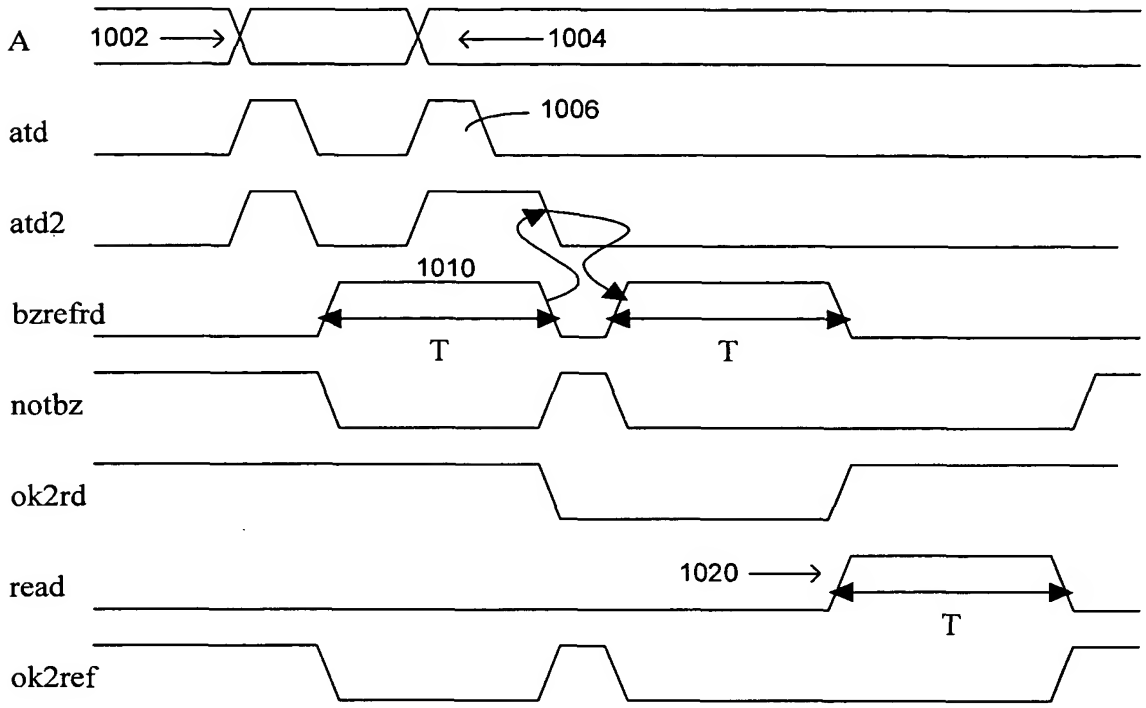

FIG. 10

Timing diagram for an invalid read operation terminated within 2*T of starting

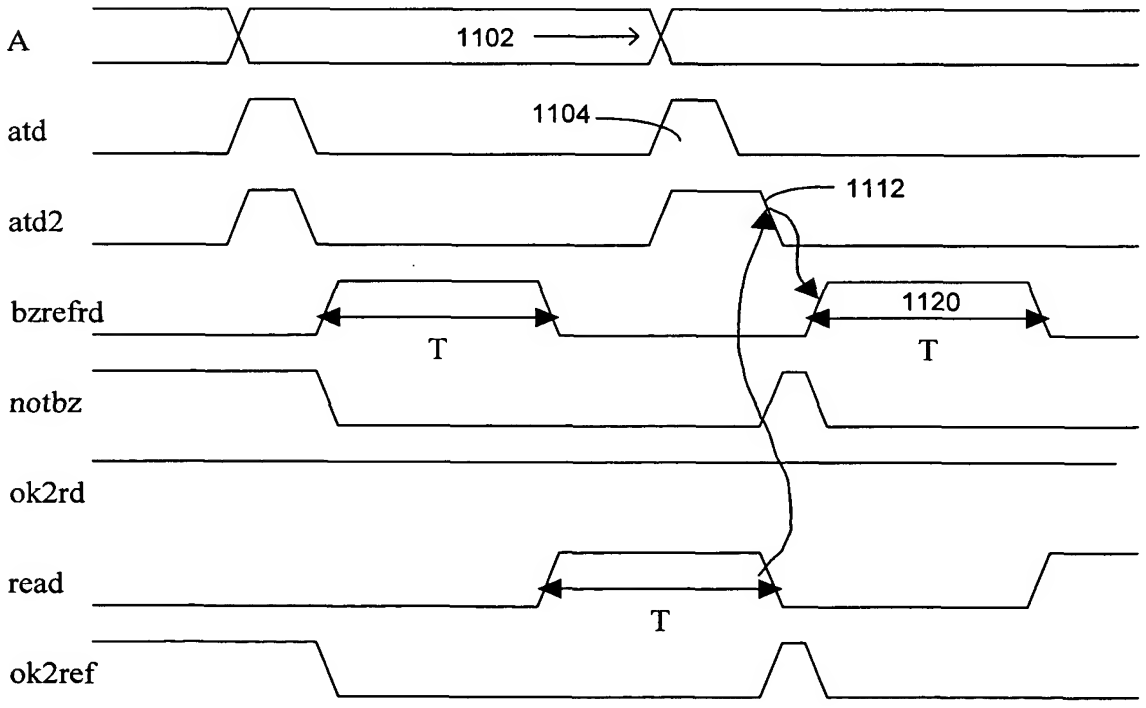

FIG. 11

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Timing diagram of a write cycle

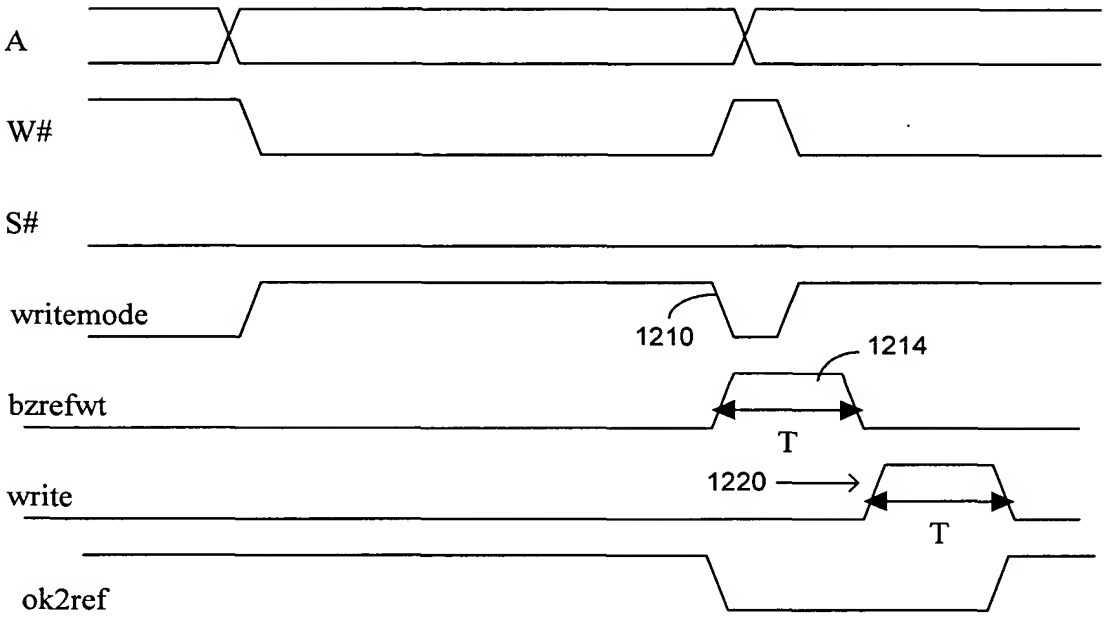

FIG. 12

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Timing diagram of a write cycle
immediately followed by a read

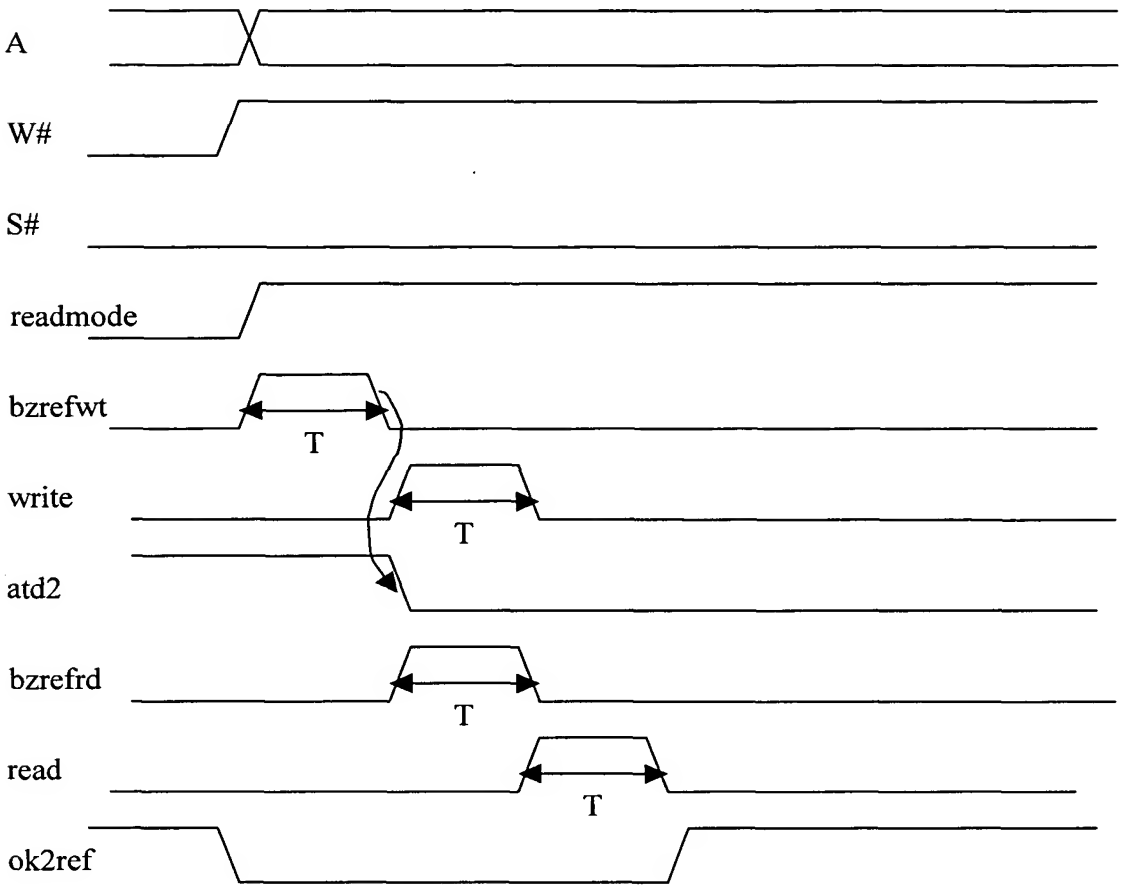

FIG. 13